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(54) **COMMUNICATION EQUIPMENT**

(57) Abstract:

PROBLEM TO BE SOLVED: To reduce the scale of hardware by dividing modulation and demodulation processing in a base band part for every processing unit and processing plural channels in divided arithmetic units in time-multiplexing manner.

SOLUTION: Symbol period arithmetic engines 403 are plurally provided in parallel or a slot period arithmetic engine 405 is operated faster than a frame period arithmetic engine 407. A block required for modulation/ demodulation processing is divided into each processing unit to allow the processing blocks to operate independent from each other. In addition, the received signals of the base band are stored in a first buffer memory 402 by the portion of several times of one symbol being the processing unit of the engine 403. Each engine is controlled by a control engine 401 and the respective engines 403, 405 and 407 asynchronously execute modulation/demodulation processing by the engine 401 and a channel to be processed is independent for every engine. Thus, the plural channels is highly efficiently modulated/ demodulated in time-multiplexing manner.